This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (canceled)

Claim 2 (new): A semiconductor integrated circuit device comprising:

a fuse cell array;

fuse cells arranged in the fuse cell array, the fuse cells including erasable and programmable nonvolatile memory cells;

a fuse cell data program and erase circuit which programs fuse data to the erasable and programmable nonvolatile memory cells and erases the fuse data from the erasable and programmable nonvolatile memory cells;

a fuse cell data control circuit which controls read out timing of the fuse data stored in the erasable and programmable nonvolatile memory cells, based on a first signal generated upon detection of power-on; and

fuse data latch circuits which latch the fuse data read out from the erasable and programmable nonvolatile memory cells.

Claim 3 (new): The device according to claim 2, wherein the erasable and programmable nonvolatile memory cells each have a gate electrode, a source region, and a drain region.

Claim 4 (new): The device according to claim 3, wherein each of the gate electrodes is connected to a word line, each of the source regions is connected to a source line, and each of the drain regions is connected to a bit line.

Claim 5 (new): The device according to claim 4, wherein each bit line is connected to the fuse cell data program and erase circuit and the fuse data latch circuits.

Claim 6 (new): The device according to claim 5, wherein the fuse data is supplied to each bit lines from the erasable and programmable nonvolatile memory cells during a read mode, and the

fuse data is supplied to each bit line from the fuse cell data program and erase circuit during a write mode and an erase mode.

Claim 7 (new): The device according to claim 6, wherein a second signal is supplied to the source line and a voltage of the second signal varies depending on which of the read mode, the write mode, and the erase mode is active.

Claim 8 (new): The device according to claim 2, wherein the fuse data contains operation/function setting information.

Claim 9 (new): The device according to claim 8, wherein the operation/function setting information is erasable and programmable.

Claim 10 (new): The device according to claim 9, wherein the operation/function setting information includes at least any one of

(a) redundancy information,
(b) write/erase inhibit block information,
(c) bit configuration information,
(d) pad location information,
(e) TOP BOOT/BOTTOM BOOT information, and
(f) information for inhibiting use of an internal test circuit.

Claim 11 (new): The device according to claim 10, wherein the write/erase inhibit block information is user-modifiable.

Claim 12 (new): The device according to claim 10, wherein the bit configuration information is user-modifiable.

Claim 13 (new): The device according to claim 10, wherein the TOP BOOT/BOTTOM BOOT information is user-modifiable.